Burak Biyikli

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Education

M.S. Electrical & Computer Engineering *8/2022 - 5/2025*
The University of Texas at Austin, GPA: 3.87, Track: Computer Architecture

B.S. Electrical Engineering *8/2018 - 1/2022*
The University of Texas at Austin, GPA: 3.83, Track: Integrated Circuits

B.A. Mathematics *1/2021 - 1/2022*
The University of Texas at Austin, GPA: 3.80, Track: Mathematics

Relevant Coursework: *Microarchitecture, Prediction Mechanisms, System on Chip (SOC) Design, Digital Systems Design, Computer Architecture: Parallelism and Locality, VLSI, Parallel Computer Architecture, High Speed Computer Arithmetic, Computer Architecture*

Projects

x86 CPU: 16 Rank OoO DRAM controller, double pumped bus, 6 stage pipeline, 1 cycle cache
Synthesis Tool: Delay minimized structural verilog from FSMs, PLA, BLIF, C-like expressions
Custom CPU: Microcoded 8-bit CMOS, 2494 mosfets/2 ROMs, 5 addressing modes, 16 GPIOs
LC3B/C CPU: Cycle accurate model of the Microcoded/Pipelined LC3B reference design
Trace Based Cache Sim: Multicore traces from Intel PT, multilevel cache, tracked coherence
MCU 3D graphics engine: 32KB RAM+ROM, 600 triangles, lighting, 25 FPS, 80MHz Arm M4F
Other Projects: 16:16 Clos Network Interconnect, RISC ALU, Verilog serial block, MCU GPS

Work Experience

The University of Texas at Austin — Austin, Texas *01/2021 - Present*
Embedded Graduate Teaching Assistant

- Instructed 330+ upper division embedded design students covering topics like: firmware development, SOC architecture, serial interfaces, power circuits, and PCB layout.
- Updated course to use tools like GitHub, KiCad, MQTT, Code Composer Studio, and Eagle.
- Mentored student projects, giving firmware/hardware/system design guidance for projects such as: Gameboy emulator, haptic feedback mouse, 3D printer, and Robot Dog.

The University of Texas at Austin — Austin, Texas *08/2022 - 12/2024*
FAST Graduate Research Assistant

- Contributed to the Primate research project, which focused on high-level synthesis, FPGA overlays, accelerator design, and compiler generation.
- Extended Primate's RTL/HLS to develop a REGEX accelerator. Refactored code to create test infrastructure, integrate performance counters, and add debug instrumentation.
- Containerized Primate by determining existing dependencies present on the group's golden copy, while reducing the complexity of its build scripts and tooling.

Texas Instruments — Santa Clara, California *05/2023 - 08/2023*
CPP Digital Logic Design Intern

- Developed a Python based RTL generation tool that produced finalized digital blocks which included: synthesizable Verilog, test benches, test cases, lint scripts, assertions, and wiring macros. This reduced engineering time per design by a couple weeks while also reducing the risk of design errors.

- Independently created and iterated multiple versions of the timer generation tool. Incorporated feedback from the design team to integrate the tool into the existing FSM generation flow. Authored comprehensive usage/architecture/timing documentation for the tool to enable interoperability.
- Explored power reduction techniques and error tolerance for generated counters. Used simulation to guide minimization of power consumption. Used LFSRs to reduce area.

Texas Instruments — Santa Clara, California *05/2021 - 08/2022*

CPP DMS Design Verification Intern

- Created and verified behavioral models of analog blocks (ILIM, Inductor, and Converter) in SystemVerilog EEnets and Verilog AMS for digital-centric mixed-signal design verification to deliver 10-100x speedup. This speedup was required to meet customer milestones.
- Created a program to quickly (~1-30 seconds) and automatically parse, process, modify, annotate, and view large simulation databases (+200GB) using Python and Cadence config files to create customer facing documents.

Texas Instruments — Dallas, Texas *05/2020 - 08/2020*

Central Analog Engineering Intern

- Validated 'simulation for test' flow by writing a test program for a new low IQ LDO using C++ running on a virtual Eagle ETS-88 Platform. Contributed related Verilog AMS, and System Verilog matching Allegro schematics of TI's ETS-88 standard hardware, enabling adoption of the flow.
- Solicited feedback from teams outside CAE to add key features and automation to TI's test engineering flow. Organized a group of interns to complete projects addressing identified shortcomings and requested features for the flow.

Advanced Micro Devices — Austin, Texas *05/2019 - 08/2019*

Application Test Equipment & Silicon Level Test Engineer Intern

- Ported feature to re-enable test time reduction in smartest with C++, Python & Advantest Firmware Commands. Test time reduction saved about $250K in the subsequent quarter.
- Worked on production code for Advantest Testers as well as Verigy’s Handlers, Firmware, APIs, prototyped changes in simulated environment. Automated tasks like the correction of limits within the test program using Python and Bash. This automation saved hours of engineering time per product.

Silicon Labs — Austin, Texas *05/2018 - 08/2018*

Central Engineering Intern

- Automated verification of simulation 1:1 with data from fabrication partners. The tool used Python, SpectreMDL, SKILL, and Ocean scripts in order to create/run test benches, parse results, and highlight outliers that may exist.

Vast.com — Austin, Texas *05/2017 - 08/2017*

Software Development Intern

- Setup and maintained backend infrastructure. Utilized existing databases to create predictive ML models for pricing. Added tracking and piped data to existing dashboards.

Technical Skills

Hardware Description Languages: Verilog, System Verilog, Chisel, Verilog A, Verilog AMS
Programing Languages: Python, C, Java, Bash, Javascript, x86, C/C++, Scala, TCL, Rust
Verification & Simulation: SVA, UVM, Jasper Gold, Cadence Virtuoso, PrimeTime, Gem5
Tools & Platforms: Linux (RHEL, Ubuntu), Git, KiCAD, Eagle, Arm, Thumb, Champsim, ASIP