Work Experience

Texas Instruments (APP-CPP) May 2023 - Aug 2023
Digital Logic Design Intern Santa Clara, California

- Created RTL generation tool which created synthesizable Verilog, test cases, test benches, inst. & wiring macros, lint scripts, and assertions. This reduced design cycle time by days, as the output was a finalized digital block.
- Explored counters designs with simulation, to determine potential tool output
- Wrote design/architecture/timing documents for the generated RTL and the tool. Updated and maintained previously created documentation.

Texas Instruments (APP-CPP) May 2022 - Aug 2022
Digital Mixed Signal Design Verification Intern Santa Clara, California

- Created and verified behavioral models of analog blocks (ILIM, Inductor, and Converter) for digital-centric mixed-signal simulation using System Verilog, EEnet, and Verilog AMS in order to deliver 10-100x speedup improvements
- Debugged and modified System Verilog AMS Cadence Connect Modules
- Created and maintained documentation relating to topics such as model vs schematic test benches, design sync, EEnet, and new hire onboarding

Texas Instruments (APP-CPP) May 2021 - Aug 2021
Digital Mixed Signal Design Verification Intern Santa Clara, California

- Created a program to quickly (~1-30 seconds) and automatically parse, process, modify, annotate, and view large simulation databases (+200GB) using Python
- Utilized standard cadence file types in order to improve ease of adoption
- Collaborated with engineers from companies that commissioned custom silicon from TI in order to create diagrams and waveforms for TI presentations.

ECE Department of UT Austin Jan 2021 - Dec 2023
Teaching Assistant Austin, Texas

- Helped students in an upper division Embedded Systems class create projects such as: haptic feedback computer mouse, voice assistant, 3D printer driver
- Updated class material to use newer tools/tech such as Git, KiCad, and MQTT

Texas Instruments (CAE) May 2020 - Aug 2020
Product / Test Engineering Intern Dallas, Texas

- Worked with teams outside CAE to find and add features and automation to TI's test engineering flow. Organized a group of interns to complete projects addressing identified shortcomings and requested features for the flow.
- Validated TI's new 'simulation for test' flow by writing a test program for a new low I_Q LDO using C++ running on a virtual Eagle ETS-88 Platform
- Developed Verilog A, Verilog AMS, and System Verilog files based on Allegro schematics of TI's ETS-88 standard hardware, allowing easier adoption of flow

Advanced Micro Devices May 2019 - Aug 2019
ATE & SLT (Silicon Level Test) Intern Austin, Texas

- Added feature to enable test time reduction in smartest with C++, Python & Advantest Firmware Commands. Test time saved valued at a quarter-million dollars in the subsequent quarter
- Worked on production code for Advantest Testers as well as Verigy's Handlers, Firmware, APIs, prototyped changes in simulated environment
- Automated tasks like the correction of limits within the test program using Python and Bash. This automation saved hours per design.

Silicon Labs May 2018 - Aug 2018
Central Engineering Intern Austin, Texas

- Automated the simulation of devices corresponding 1:1 with measurement data given by our fabrication partner. This correlated & verified our simulations.
- Used Python to process both measured and simulated data. Worked with SpectreMDL, SKILL, and Ocean in order to accurately simulate devices.

Vast.com May 2017 - Aug 2017
Software Development Intern Austin, Texas

- Utilized existing databases to create predictive ML models for pricing
- Set up and maintained backend infrastructure

Burak Biyikli

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Education

MS Electrical & Computer Engineering (ACSES Track)
The University of Texas at Austin
2022-2024
GPA: 4.00

Ph.D. Electrical & Computer Engineering (ACSES Track)
The University of Texas at Austin
2022-2028, University Fellowship
GPA: 4.00

BS Electrical & Computer Engineering (IC Track)
The University of Texas at Austin
2018-2022, University Honors
GPA: 3.83

BA Mathematics
The University of Texas at Austin
2021-2022, University Honors
GPA: 3.80

Skills

Python, Verilog, System Verilog, SVA, Verilog A, VerilogAMS, System Verilog EEnet, Linux (RHEL, ubuntu), Git, Bitbucket, C, C++, Java, Virtuoso ADE, Eagle, KiCAD, Mathematica, Swift/Xcode, Arm, Thumb, x86

Coursework

Comp. Arch. & IC Design:
SOC Design
Comp. Arch. Parallelism & Locality
VLSI
Parallel Comp. Arch.
Analog IC Design
Computer Architecture
High Speed Comp. Arithmetic
Digital Systems Design
Solid State Electronic Devices

Embedded Systems:
Real Time Operating Systems
Technology for Embedded IOT
Embedded Systems Design Lab

Personal Projects

Custom CPU
3D Graphics Engine
Microcontroller based GPS
Smart Street light
Chess Engine