Burak Biyikli

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Education

MS Electrical & Computer Engineering (Computer Architecture)
The University of Texas at Austin, GPA: 3.87, Aug 2022 - May 2025

BS Electrical & Computer Engineering (Integrated Circuits)
The University of Texas at Austin, GPA: 3.83, Aug 2018 - May 2022

BA Mathematics (Focus Mathematics)
The University of Texas at Austin, GPA: 3.80, Jan 2021 - May 2022

Coursework: Microarchitecture, System on Chip (SOC) Design, Computer Architecture: Parallelism & Locality, VLSI, Parallel Computer Architecture, High Speed Computer Arithmetic, Digital Systems Design, Real Time (OS)

Projects

x86 CPU: 16 Rank OoO DRAM controller, 2 channel double pumped bus, 6 stage pipeline, single cycle unaligned cache
Verilog Synthesis Toolchain: Synthesizes optimized structural verilog from FSMs, truth tables, and C style expressions
Custom 8 bit CPU: Microcoded CMOS in 2494 transistors + 2 ROMs, 5 addressing modes, 18 instructions, 16 GPIOS
LC3B/C CPU: Cycle accurate C model of the LC3B (Microcoded) and LC3C (Pipelined) reference designs
MCU 3D graphics engine: Written in C, 32KB RAM+ROM, 600 triangles + lighting, 25 FPS on 80MHz Arm M4 CPU
16:16 Clos Network Interconnect, RISC ALU, verilog serial block, MCU GPS, Smart Street light, Chess Engine

Experience

Cockrell School of Engineering (UT Austin) — Austin, Texas

Research Assistant — Aug 2022 - Present
Head TA, Graduate Teaching Assistant (Embedded Systems Design Lab) — Aug 2023 - Present
Undergraduate Teaching Assistant (Embedded Systems Design Lab) — Jan 2021 - May 2022

- Worked on Primate, a research project on high-level synthesis, FPGA overlays, accelerator design, and compiler generation. Worked on the RTL/HLS aspect of the project developing a REGEX accelerator and adding perf. counters
- Containerized Primate by resolving dependencies, while reducing the complexity of its build scripts and tooling.
- Taught embedded design covering: SOC architecture, firmware development, serial interfaces, power circuits, and PCB layout. Updated materials with tools like GitHub Classroom, Eagle, KiCad, and MQTT.
- Helped create student projects: Gameboy emulator, haptic feedback mouse, ATC radio, voice assistant, 3D printer

Texas Instruments — Santa Clara, California

Digital Logic Design Intern (Custom Power Products) — May 2023 - Aug 2023
Digital Mixed Signal Design Verification Intern (Custom Power Products) — May 2021 - Aug 2022
Product / Test Engineering Intern (Central Analog Engineering) — May 2020 - Aug 2020

- Reduced design cycle time by creating a timer generator. It produced finalized digital blocks including: synthesizable Verilog, test benches/cases, lint scripts, assertions, and wiring macros. Explored power reduction avenues for timers.
- Created and verified behavioral models of analog blocks (ILIM, Inductor, and Converter) in SystemVerilog EEnets and Verilog AMS for digital-centric mixed-signal design verification to deliver 10-100x speedup.
- Created a program to quickly (~1-30 seconds) and automatically parse, process, modify, annotate, and view large simulation databases (+200GB) using Python and Cadence config files to create customer facing documents
- Developed and Validated TI's new 'simulation for test' flow by writing a test program for a new low I_Q LDO using C++ running on a virtual Eagle ETS-88 Platform, while also creating VerilogAMS library files based on Allegro Schematics of ETS-88 Standard hardware.

Advanced Micro Devices — Austin, Texas

ATE & SLT (Application and Silicon Level Test) Intern — May 2019 - Aug 2019

- Ported feature to re-enable test time reduction in smartest with C++, Python & Advantest Firmware Commands. Test time saved valued at a quarter-million dollars in the subsequent quarter
- Worked on code for Advantest Testers as well as Verigy's Handlers, Firmware, APIs. Automated tasks like the correction of limits within the test program using Python and Bash. This automation saved hours per design.

Silicon Labs — Austin, Texas

Central Engineering Intern — May 2018 - Aug 2018

- Automated verification of simulation 1:1 with data from fabrication partners. The tool used Python, SpectreMDL, SKILL, and Ocean scripts in order to create/run test benches, parse results, and highlight outliers that may exist.

Vast.com — Austin, Texas

Software Development Intern — May 2017 - Aug 2017

Skills: Verilog, System Verilog, Python, C, SVA, Verilog A, VerilogAMS, UVM, Jasper Gold, System Verilog EEnet, Linux (RHEL, ubuntu), Git, Bitbucket, C++, Java, Virtuoso ADE, Eagle, KiCAD, Arm, Thumb, x86, PrimeTime